Module 4 Computer Hardware

Module title	Computer Hardware
Module NFQ level (only if an NFQ level can be demonstrated)	n/a
Module number/reference	BSCH-CH
Parent programme(s)	Bachelor of Science (Honours) in Computing Science
Stage of parent programme	Stage 1
Semester (semester1/semester2 if applicable)	Semester 1 & 2
Module credit units (FET/HET/ECTS)	ECTS
Module credit number of units	10
List the teaching and learning modes	Direct, Blended
Entry requirements (statement of knowledge, skill and competence)	Learners must have achieved programme entry requirements.
Pre-requisite module titles	None
Co-requisite module titles	None
Is this a capstone module? (Yes or No)	No
Specification of the qualifications (academic, pedagogical and professional/occupational) and experience required of staff (staff includes workplace personnel who are responsible for learners such as apprentices, trainees and learners in clinical placements)	Qualified to as least a Bachelor of Science (Honours) level in Computer Science or equivalent and with a Certificate in Training and Education (30 ECTS at level 9 on the NFQ) or equivalent.with a Certificate in Training and Education (30 ECTS at level 9 on the NFQ) or equivalent.
Maximum number of learners per centre (or instance of the module)	60
Duration of the module	Two Academic Semesters, 24 weeks teaching
Average (over the duration of the module) of the contact hours per week	4.5
Module-specific physical resources and support required per centre (or instance of the module)	One class room with capacity for 60 learners along with one hardware lab with capacity for 25 learners for each group of 25 learners

Analysis of required learning effort		
	Minimum ratio teacher / learner	**Hours**
Effort while in contact with staff		
Classroom and demonstrations	1:60	60
Monitoring and small-group teaching	1:25	36
Other (specify)		
Independent Learning		
Directed e-learning		
Independent Learning		97
Other hours (worksheets and assignments)		57
Work-based learning – learning effort		
Total Effort		250

Allocation of marks (within the module)					
	Continuous assessment	**Supervised project**	**Proctored practical examination**	**Proctored written examination**	**Total**
Percentage contribution	50%			50%	100%

Module aims and objectives

Learners are helped to develop their knowledge and understanding of how computer hardware is constructed and how the hardware can be made to implement logic and arithmetic and to run programs. Since computing is showing itself to be both pervasive and fast evolving, the module emphasizes the key principles that continue to apply while allowing the scope of the learning to benefit from the broad base envisaged in the module.

Learners are expected therefore to apply the principles of computer hardware to both current and developing technologies. Further, they are helped to cultivate an understanding of how the insights and practice from computer hardware technology contribute to the current state of the art in the wider Computer Science landscape.

Minimum intended module learning outcomes

On successful completion of this module, the learner will be able to:

1. Compare and contrast approaches to computer architecture
2. Explain how data is encoded
3. Solve problems of combinational and sequential logic
4. Examine the role and construction of key hardware components and explain how they operate
5. Explain the role played by storage and analyse and compare approaches to storage

6. Explain how processing is carried out and review the factors that influence processing performance
7. Explain how to construct and program a microcontroller system which includes input and output components
8. Create simple programs in assembly language that target a microcontroller platform

Rationale for inclusion of the module in the programme and its contribution to the overall MIPLOs

This module aims to support learners as they develop their understanding of how computing machines are implemented. The topics covered and the manner in which they are dealt with is intended to be broadly based so as to lay a solid foundation of learning. Particular attention is paid to the application of digital logic in combinational and sequential logic components that implement counting, arithmetic and logic functions. This theme is developed further with a focus on key components such as the processor and memory and the interaction of these components with simple programs.

Learners develop an awareness of current technologies, literature and research in the area. Learners are expected to apply the principles of computer hardware to both current and developing technologies. Further, they cultivate an understanding of how the insights and practice from computer hardware technology contribute to the current state of the art in the wider Computer Science landscape. Appendix 1 of the programme document maps MIPLOs to the modules through which they are delivered.

Information provided to learners about the module

Learners receive a programme handbook to include module descriptor, module learning outcomes (MIMLO), class plan, assignment briefs, assessment strategy and reading materials.

Module content, organisation and structure

Data encoding and number bases

- How computer hardware encodes data.
- The number bases of relevance in computing.
- Converting numerical data from one number base to another

Digital logic

- Logic circuits, their truth tables and equations.
- Design and simplification of logic circuits using Boolean algebra and Karnaugh-Veitch maps
- Sequential logic, excitation tables, state tables and state diagrams.

- Shift registers and counters.
- Arithmetic logic unit construction and operation.
- Logic components such as the half-adder, adder, comparator and decoder.

Computer Architectures, Processing & Programming

- Von Neumann and Harvard architectures. Processor design approaches
- Techniques for performance enhancement such as caching and parallelism.
- Computer mainboard components such as the processor, buses and bus bridging chips, ports, network and graphics chips.
- Instruction execution.
- Writing simple programs in assembly language.
- Comparisons between assembly language mechanisms like branching and higher-level programming constructs such as conditional statements and iteration.

Storage

- The need for different types of storage.
- Hierarchical models such as the storage pyramid.
- Storage cell construction.
- How primary storage impacts processing performance.
- Caching.
- Secondary storage devices.
- Access times and transfer rates for secondary storage devices.
- Redundancy based systems such as RAID.

Number Representation

- Unsigned integer representation.
- Sign and magnitude representation and two's complement representation.
- Fixed point number representation.
- Floating point number representation.

Input & Output

- Input and output devices.
- Serial and parallel movement of data.
- Movement of data to and from devices.
- Interrupts and polling.

Embedded Systems

- Embedded system architectures and applications.
- Typical hardware and software.
- Tools.
- Hardware construction and the connection of input (including sensors) and output components (indicators/actuators).
- Creating and uploading programs in assembly language and C.
- Debugging an embedded system consisting of hardware and software.

Module teaching and learning (including formative assessment) strategy
The module is delivered through a combination of lectures, tutorials, and practical lab sessions. The tutorials and practical lab sessions reinforce the learning in lectures. The emphasis is on developing knowledge and understanding in context.

Assessment is divided into four elements. The continuous assessment consists of a series of take home assignments. These assess the learner's competency in specific areas of the syllabus. Finally, there is an end of semester exam that tests the learners understanding of the theoretical material.

Timetabling, learner effort and credit
The module is timetabled as two 1.5-hour lectures and one 1.5-hour lab per week.

The number of 10 ECTS credits assigned to this module is our assessment of the amount of learner effort required. Continuous assessment spreads the learner effort to focus on small steps before integrating all steps into the overall process of computer program design and implementation.

There are 108 contact hours made up of 48 lectures delivered over 24 weeks with classes taking place in a classroom. There are also 24 lab sessions delivered over 24 weeks taking place in a fully equipped hardware lab. The learner will need 85 hours of independent effort to further develop the skills and knowledge gained through the contact hours. An additional 57 hours are set aside for learners to work on worksheets and assignments that must be completed for the module. The team believes that 250 hours of learner effort are required by learners to achieve the MIMLOs and justify the award of 10 ECTS credits at this stage of the programme.

Work-based learning and practice-placement
There is no work based learning or practice placement involved in the module.

E-learning
The college VLE is used to disseminate notes, advice, and online resources to support the learners. The learners are also given access to Lynda.com as a resource for reference.

Module physical resource requirements
Requirements are for a classroom for 60 learners equipped with a projector, and a 20-seater hardware lab for practical sessions with access to various circuit building equipment and several machines for the development of assembly code.

Recommended Text

Harris, S. L. and Harris, D. M. (2016) *Digital Design and Computer Architecture*. Amsterdam: Elsevier.

Secondary Reading

Clements, A. (2006) *Principles of Computer Hardware*. Oxford: Oxford University Press

Floyd, T. L. (2015) *Digital Fundamentals*. Harlow: Pearson.

Kleitz, W. (2014) *Digital Electronics: A Practical approach with VHDL*. Harlow: Pearson Education.

Null, L. and Lobur, J. (2015) *The Essentials of Computer Organization and Architecture*. Burlington: Jones & Bartlett Learning.

Smith, D. W. and Smith, D. W. (2006) *PIC in Practice: a Project-based Approach*. Oxford: Elsevier.

Stallings, W. (2018) *Computer Organization and Architecture: Designing for Performance*. Hoboken: Pearson Education.

Wilmshurst, T. (2011) *Designing Embedded Systems with PIC Microcontrollers: Principles and Applications*. London: Newnes

Specifications for module staffing requirements

For each instance of the module, one lecturer qualified to at least Bachelor of Science (Honours) in Computer Science or equivalent, and with a Certificate in Training and Education (30 ECTS at level 9 on the NFQ) or equivalent.with a Certificate in Training and Education (30 ECTS at level 9 on the NFQ) or equivalent.. Industry experience would be a benefit but is not a requirement.

Learners also benefit from the support of the programme Director, programme administrator, learner representative and the Student Union and Counselling Service.

Module Assessment Strategy

The assignments constitute the overall grade achieved, and are based on each individual learner's work. The continuous assessments provide for ongoing feedback to the learner and relates to the module curriculum.

No.	Description	MIMLOs	Weighting
1	A take home assignment based on elements of the theoretical aspects of the module.	1-6	10%
2	A take home assignment based on elements of the theoretical aspects of the module.	1-6	20%

3	A take home assignment based on elements of the theoretical aspects of the module.	1-8	20%
4	Written exam that tests the theoretical aspects of the module	1-8	50%

All repeat work is capped at 40%.

Sample assessment materials

Note: All assignment briefs are subject to change in order to maintain current content.

Assignment 1

Answer the questions numbered from 1 to 10 below. Show all working, especially in calculation/number conversion problems. All questions carry equal marks:

1. Explain why the base 2 number system is of special relevance in Computer Science.
2. Draw the schematic symbol for a NPN bipolar junction transistor. Explain why the transistor was key to the proliferation of computers and computing devices. Outline one disadvantage of using bipolar junction type transistors in logic devices.
3. Draw a diagram of a two input AND gate together with the corresponding truth table. With the help of a schematic diagram, show how AND might be implemented using discrete transistors.
4. Draw a diagram of a two input OR gate together with the corresponding truth table. With the help of a schematic diagram, show how OR might be implemented using discrete transistors.
5. Simplify, using the laws of Boolean algebra: AB + AB + ABC + AC
6. Draw the combinational logic circuit to implement the Boolean expression:

   $$Y = ACF + ACF$$

   Use Boolean algebra to simplify the expression and draw a diagram to show the simplified implementation.
7. Convert to binary:
   (a) EB4
   (b) 5D
8. Convert to hexadecimal:
   (a) 11000101
   (b) 101101001010
9. Convert to decimal:
   (a) 1011 1100
   (b) 0010 1101
10. Convert the following octal numbers to decimal:
    (a) 162
    (b) 144

Assignment 2

Introduction

Answer the questions numbered from 1 to 10 below. The work must be your own and you must show all working for each problem:

1. An ADC0804 chip is connected to a sensor that outputs a voltage in the range 0V to 5V. The A-D reference voltage is the same as the supply voltage at 5V. Show how the resolution in Volts is calculated.

2. Outline two limitations of the sign and magnitude approach to the representation of signed integers.

3. Convert to 8-bit two's complement:

(a) 123

(b) -63

4. Convert the following two's complement numbers to decimal:

(a) 1111 1001

(b) 0110 0000

5. With the help of a diagram, explain how the IEEE 754 approach represents single precision floating point numbers.

6. Show how -35.5625 is represented using the IEEE 754 approach.

7. With the help of a labelled diagram, show how the S-R flip-flop can be gated with the addition of further logic gates to control the inputs to the flip-flop.

8. (a) Write the characteristic equation and the excitation table for the T flip-flop.

(b) Write the characteristic equation and the excitation table for the J-K flip-flop.

9. With the help of a diagram and function table, explain how half adders can be combined to form a full adder.

10. With the help of a diagram, explain how a two's complement adder/subtracter can be created by combining a 4-bit full adder with a controlled inverter.

Assignment 3

Tasks

Answer the questions numbered from 1 to 10 below. This is an individual assignment. The work must be your own and you must show all working for each problem. Where you have used other sources to support your work, these must be fully referenced.

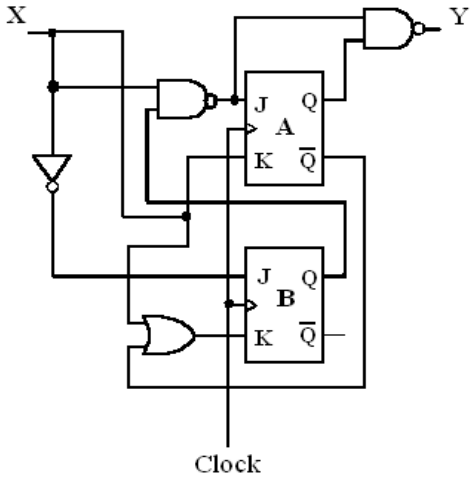

Figure 1. Sequential logic circuit

1. Write the input and output equations for the sequential logic circuit in Figure 1.

2. Write the state table for the sequential logic circuit in Figure 1.

3. Draw the state diagram for the sequential logic circuit in Figure 1.

4. Write the characteristic equation and excitation table for a T flip-flop.

5. Use a Karnaugh map to minimize the following SOP expression:

$$Y = A'B + A'B'C' + ABC' + AB'C'$$

6. Draw a fully labelled diagram of the computer storage pyramid. Explain the concepts that it illustrates.

7. Distinguish clearly between DRAM and SRAM.

8. Explain, with the help of a diagram how a PIC16F684 microcontroller may be configured with a 4MHz crystal clock to drive a LED connected to PORTC,1.

9. Write an assembly language program to drive an LED connected to PORTC,1 of a PIC16F684 microcontroller. Include a delay routine in your program so the LED on/off phases are clearly visible.

10. Draw a diagram to show a logical view of a 1 of 4 (4 channel) multiplexer/data selector with active high enable. Show the function table for the multiplexer.

GRIFFITH COLLEGE DUBLIN

QUALITY AND QUALIFICATIONS IRELAND

EXAMINATION

COMPUTER HARDWARE

Lecturer(s):

External Examiner(s):

Date: **XXXXXXXX** **Time:** **XXXXXXX**

THIS PAPER CONSISTS OF FIVE QUESTIONS
FOUR QUESTIONS TO BE ATTEMPTED
ALL QUESTIONS CARRY EQUAL MARKS

THE USE OF NON PROGRAMMABLE CALCULATORS IS PERMITTED DURING THIS EXAMINATION

QUESTION 1

(a) A material or device that is capable of two states could be considered for the purpose of building computer storage. For example, paper was used to make punched cards. Magnetism and optics have also been used. As well as the requirement of having two states, itemise two further requirements of a material or device that would make it a candidate for the purpose of computer storage.

(2 marks)

(b) A pyramid model is frequently used to illustrate the different types of storage that are used in computing. Show the pyramid storage model and label it main features. Explain the key ideas that are communicated by the pyramid storage model.

(5 marks)

(c) A certain processor has the capability to output a completed instruction every 2 nanoseconds. What is the theoretical instruction shortfall incurred by having to wait during the rotational latency of a spinning platter hard disk with a spin speed of 7200 r.p.m?

(8 marks)

(d) Interrupt and polling based approaches are both used to service peripheral devices.

(i) Compare the key differences between these approaches, highlighting any limitations.

(ii) Explain what happens when an interrupt is signalled up to the point where the interrupted task is resumed.

(10 marks)

Total (25 marks)

QUESTION 2

(a) Perform the following number conversions:

(i) Convert from binary to hexadecimal: 1110 1100 1111 1011

(ii) Convert from hexadecimal to binary: D239

(2 marks)

(b) Explain how 8-bit two's complement can be used to represent -35 (negative thirty five).

(5 marks)

(c) With the help of a diagram, explain how real numbers are represented in the IEEE 754 Single Precision Floating Point Number approach.

(8 marks)

(d) Draw a diagram to show the bit pattern that represents 56.125 using the IEEE 754 Single Precision Floating Point Number approach.

(10 marks)

Total (25 marks)

QUESTION 3

(a) Write the Identity laws of Boolean algebra.

(2 marks)

(b) An ADC0804 chip is an analog to digital (A-D) converter with 8-bit output. Pin 9 is left unconnected and the 5V supply voltage is used as the reference voltage (Vref). What output would you expect to see if pin 7 (V_{in} analog negative) is connected to 0V and 1.0V is applied to the analog input (pin 6)?

(5 marks)

(c) The logic circuit in Figure 1 has inputs A and B and output Y. Derive the equation for this logic circuit.

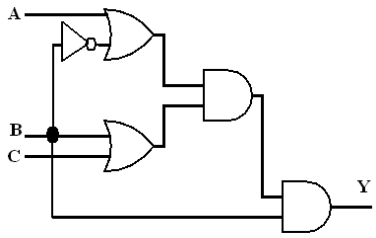

Figure 1. Logic circuit

(8 marks)

(d) Use Boolean algebra to simplify the logic expression for the circuit in Figure 1. Use the simplified expression to create an equivalent circuit with fewer logic gates.

(10 marks)

Total (25 marks)

QUESTION 4

(a) With the help of a labelled diagram, show how logic gates might be connected to create a 4-bit equality comparator.

(2 marks)

(b) With the help of a diagram show how logic gates can be connected to add two bits and support a carry in and carry out.

(5 marks)

(c) With the help of a diagram, show how J-K flip-flops can be used to create a 4-bit asynchronous counter.

(8 marks)

(d) An 8 channel (1 of 8) multiplexer has an active low enable and a 3-bit channel select interface. Channel selection is from Y0 to Y7 which can then be multiplexed/de-multiplexed onto input/output Z. Five incomplete rows from the function table of such an 8 channel multiplexer are shown in Table 1. Complete each row of the function table.

Inputs				**Channel**
Enable	**S2**	**S1**	**S0**	
L	L	H	H	
L				Y5 - Z
L				Y6 - Z
L	H	H	H	
H				

Table 1. Five incomplete rows from the function table of an 8 channel multiplexer

(10 marks)

Total (25 marks)

QUESTION 5

(a) Distinguish clearly between positive edge and negative edge triggering.

(2 marks)

(b) Write the characteristic equation and excitation table for a J-K flip flop.

(5 marks)

(c) Write the input and output equations for the circuit shown in Figure 2.

(8 marks)

(d) Write the state table and draw the state diagram for the circuit in Figure 2.

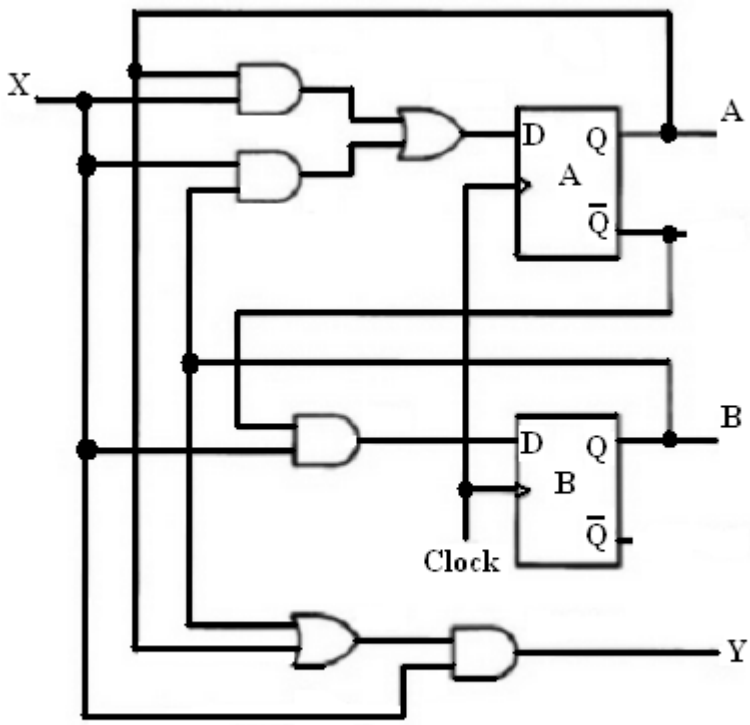

Figure 2. Sequential logic circuit

(10 marks)

Total (25 marks)